

1A: LIQUID CRYSTAL PANEL

FIG. 1

The diagram illustrates a multi-channel A/D converter system. At the top left, a box labeled '20' represents the 'CLOCK GENERATING CIRCUIT', which outputs a common clock signal 'CLK'. This 'CLK' signal is distributed to three parallel processing channels. Each channel is controlled by a specific sampling pulse: 'SP₁' for the first channel, 'SP₂' for the second, and 'SP_N' for the N-th channel. Each channel consists of an 'A/D CONVERSION TIMING CONTROL CIRCUIT' (labeled 21-1, 21-2, and 21-N respectively). These control circuits receive their respective sampling pulses and the common 'CLK'. The output of each timing control circuit is connected to an 'ADC' (labeled 16-1, 16-2, and 16-N) and a 'LATCH' (labeled 17-1, 17-2, and 17-N). The 'LATCH' blocks are connected to the outputs of the ADCs and also receive the common 'CLK' signal. The outputs of the latches are connected to the system output lines.

FIG. 2

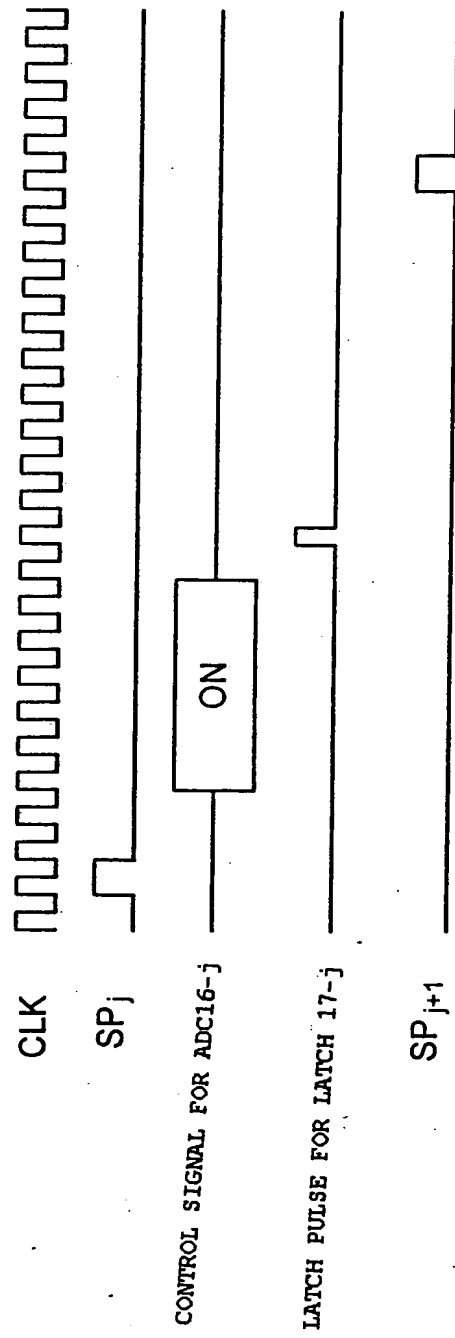


FIG. 3

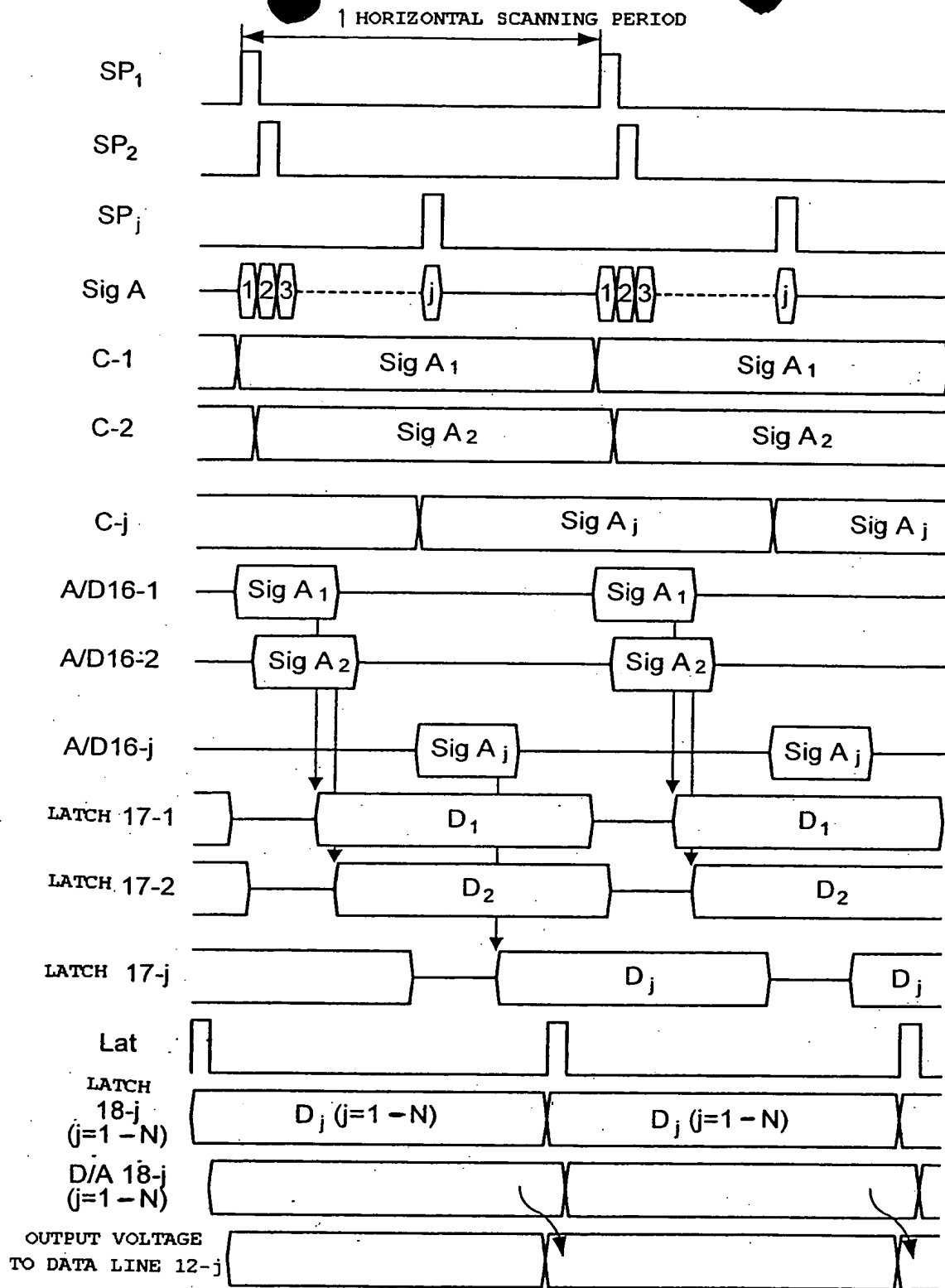


FIG. 4

66	
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09689658 101300

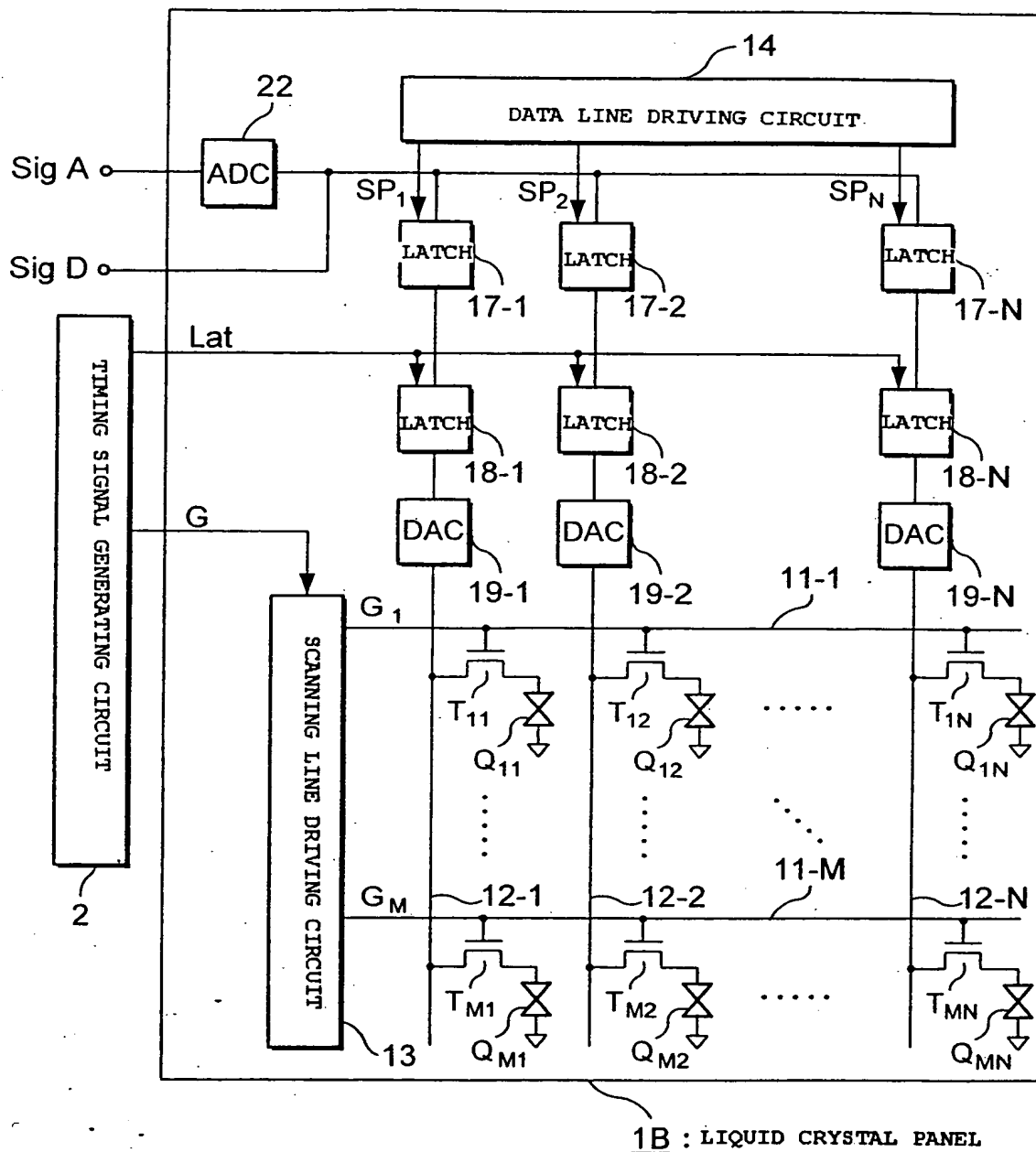


FIG. 6

00639658 101300

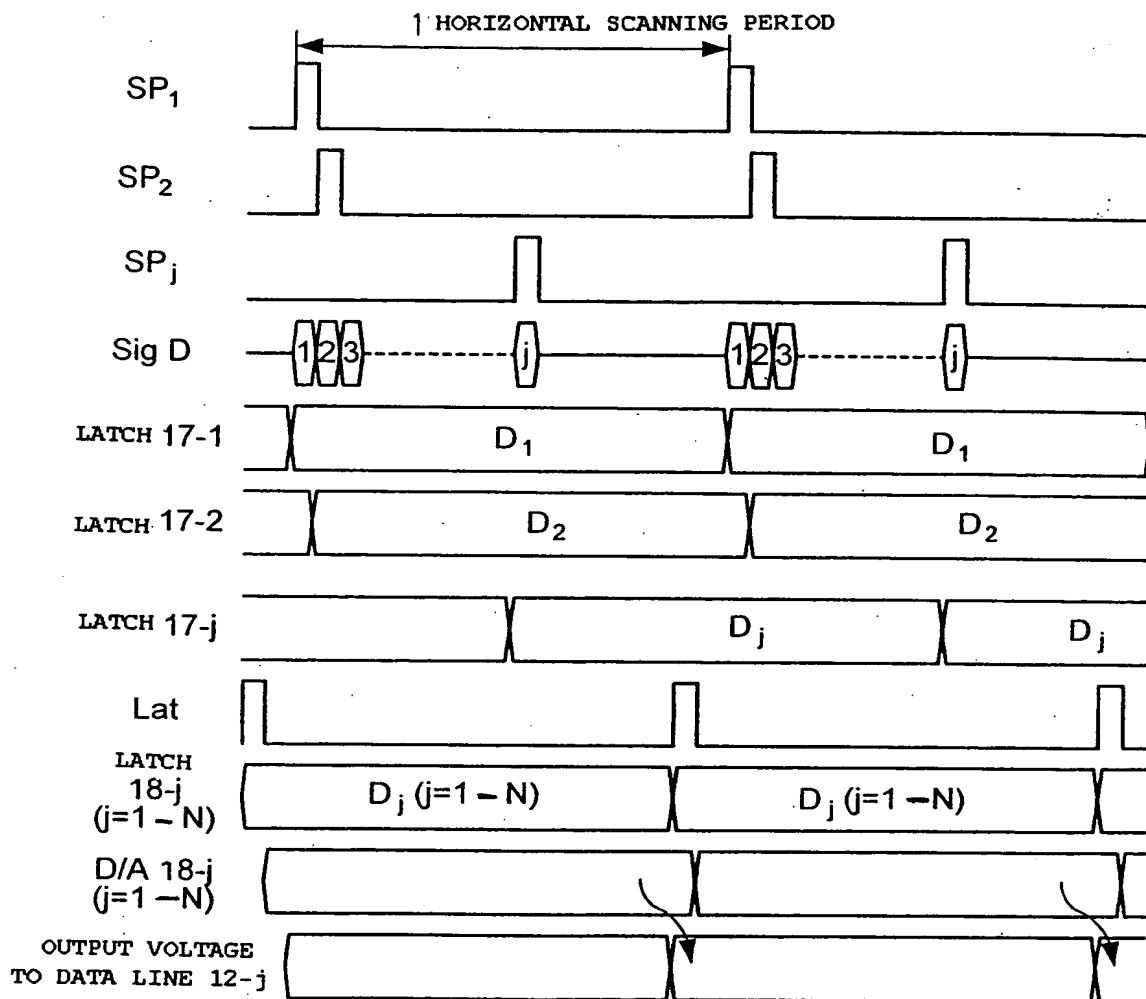
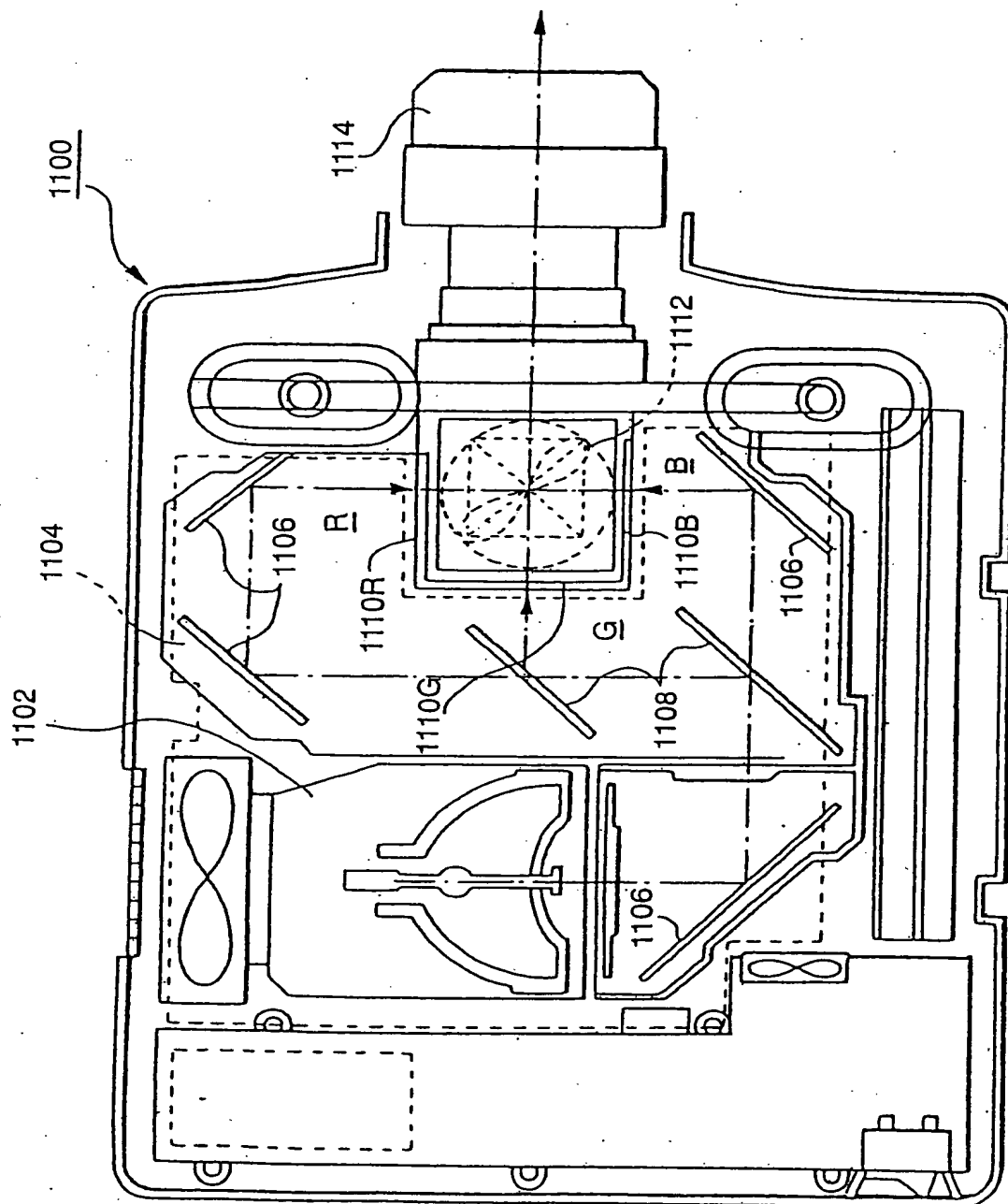


FIG. 7


$$\frac{\infty}{b}$$

1204



1200

1206

1202

09689558-101300

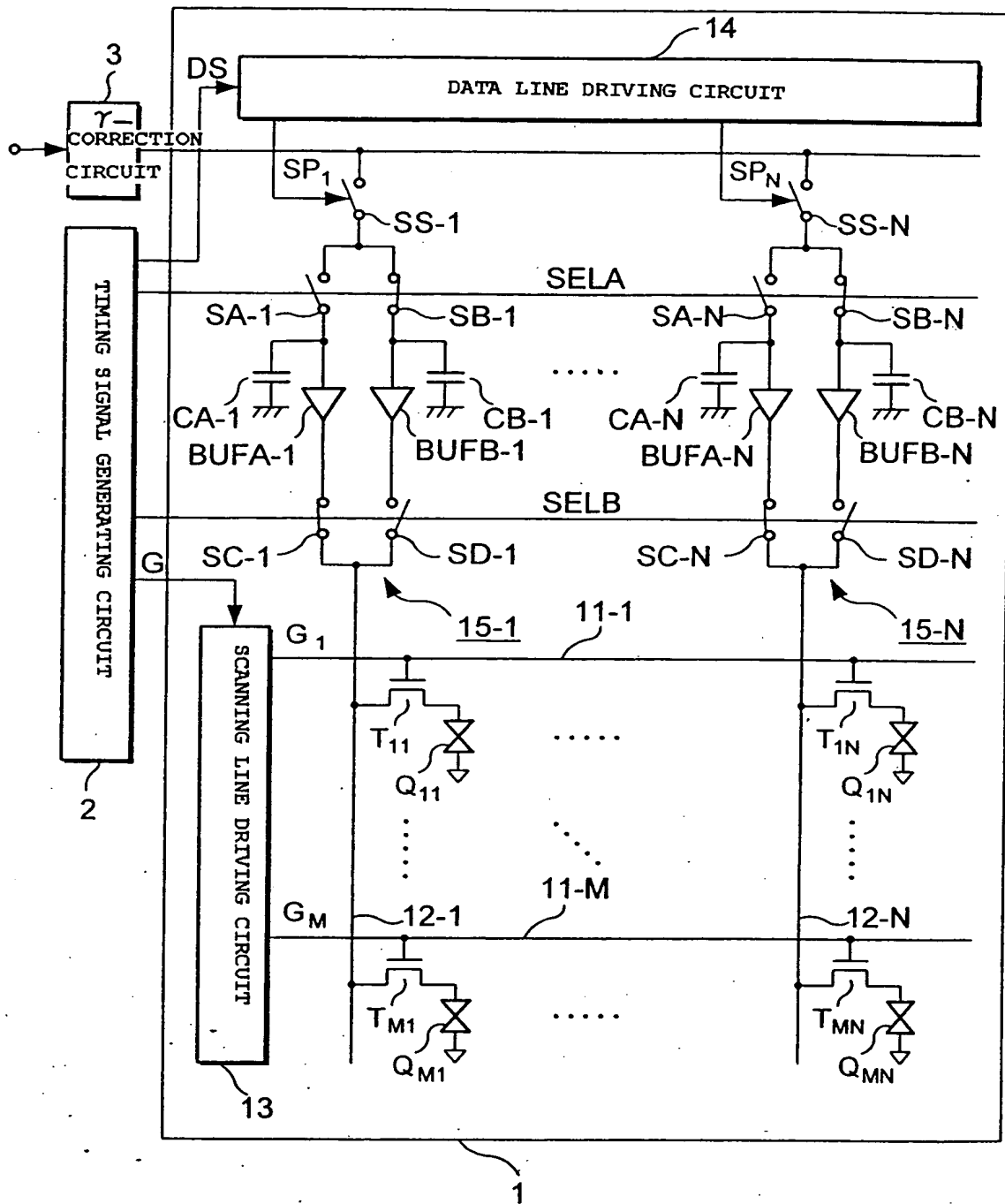


FIG. 10

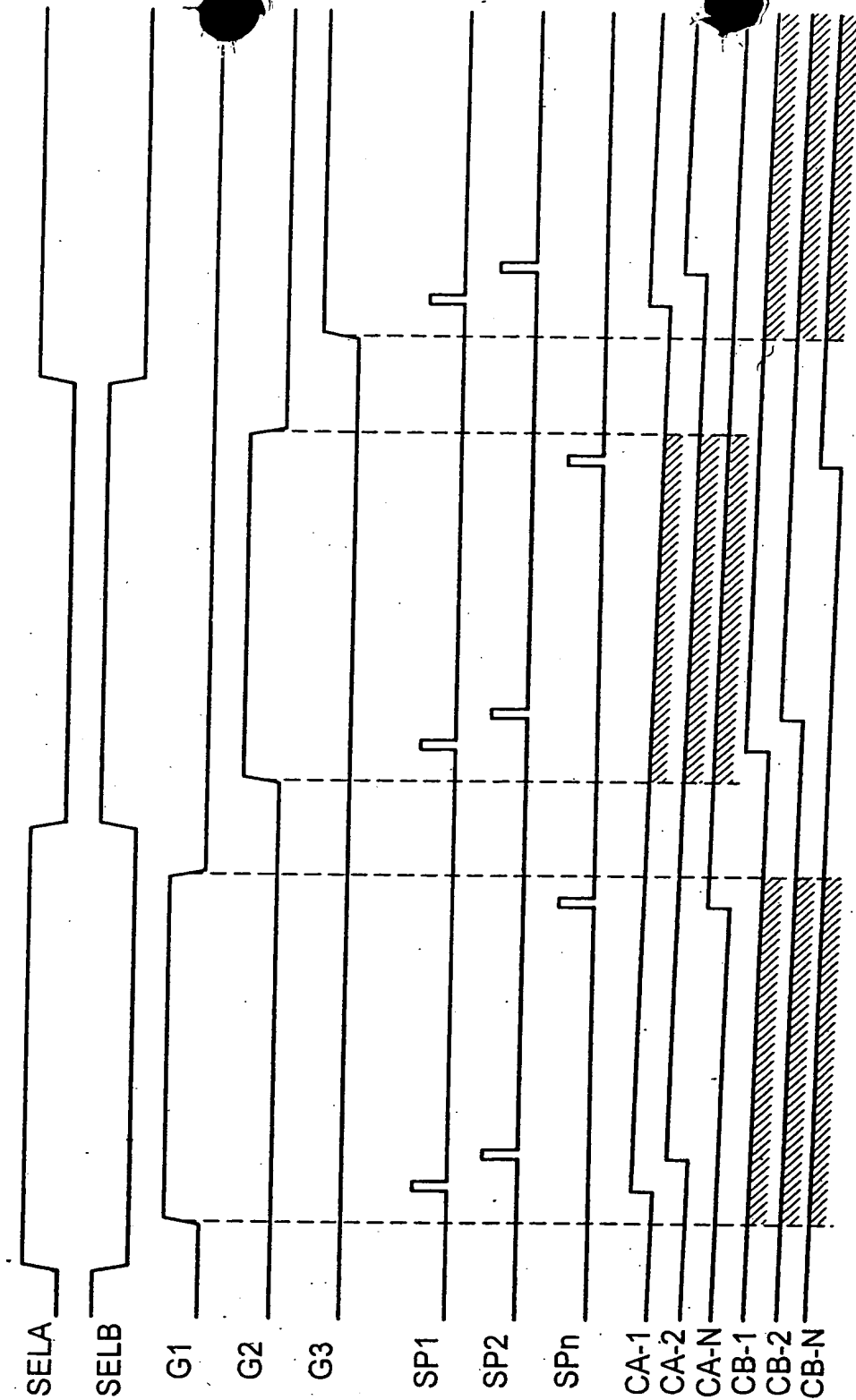


FIG. 11